

November 1994

# 54F74F109 Dual JK Positive Edge-Triggered Flip-Flop

## General Description

The 'F109 consists of two high-speed, completely independent transition clocked JK flip-flops. The clocking operation is independent of rise and fall times of the clock waveform. The JK design allows operation as a D flip-flop (refer to 'F74 data sheet) by connecting the J and  $\bar{K}$  inputs.

Asynchronous Inputs:

LOW input to  $\bar{S}_D$  sets Q to HIGH level

LOW input to  $\bar{C}_D$  sets Q to LOW level  
Clear and Set are independent of clock  
Simultaneous LOW on  $\bar{C}_D$  and  $\bar{S}_D$  makes both Q and  $\bar{Q}$  HIGH

## Features

- Guaranteed 4000V minimum ESD protection.

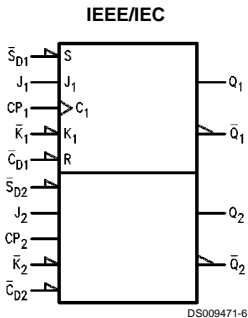
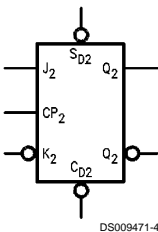
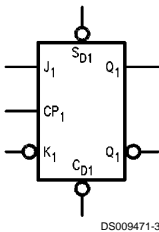
Ordering Code: See Section 0

| Commercial        | Military          | Package Number | Package Description                               |
|-------------------|-------------------|----------------|---|
| 74F109PC          |                   | N16E           | 16-Lead (0.300" Wide) Molded Dual-in-Line         |
|                   | 54F109DM (Note 2) | J16A           | 16-Lead Ceramic Dual-in-Line                      |
| 74F109SC (Note 1) |                   | M16A           | 16-Lead (0.150" Wide) Molded Small Outline, JEDEC |
| 74F109SJ (Note 1) |                   | M16D           | 16-Lead (0.300" Wide) Molded Small Outline, EIAJ  |
|                   | 54F109FM (Note 2) | W16A           | 16-Lead Cerpack                                   |
|                   | 54F109LM (Note 2) | E20A           | 16-Lead Ceramic Leadless Chip Carrier, Type C     |

Note 1: Devices also available in 13" reel. Use suffix = SCX and SJX.

Note 2: Military grade device with environmental and burn-in processing. Use suffix = DMQB, FMQB and LMQB.

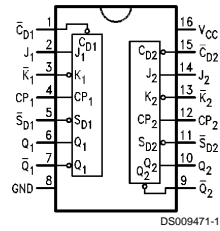
## Logic Symbols



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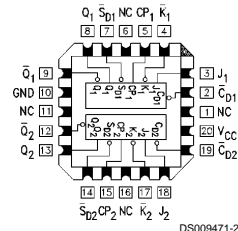
## Connection Diagrams

Pin Assignment  
for DIP, SOIC and Flatpak



DS009471-1

Pin Assignment  
for LCC



DS009471-2

## Unit Loading/Fan Out

See Section 0 for U.L. definitions

| Pin Names                        | Description                             | 54F/74F          |   |
|----------------------------------|---|------------------|---|
|                                  |   | U.L.<br>HIGH/LOW | Input $I_{IH}/I_{IL}$<br>Output $I_{OH}/I_{OL}$ |
| $J_1, J_2, \bar{K}_1, \bar{K}_2$ | Data Inputs                             | 1.0/1.0          | 20 $\mu A$ / -0.6 mA                            |
| $CP_1, CP_2$                     | Clock Pulse Inputs (Active Rising Edge) | 1.0/1.0          | 20 $\mu A$ / -0.6 mA                            |
| $\bar{C}_{D1}, \bar{C}_{D2}$     | Direct Clear Inputs (Active LOW)        | 1.0/3.0          | 20 $\mu A$ / -1.8 mA                            |
| $\bar{S}_{D1}, \bar{S}_{D2}$     | Direct Set Inputs (Active LOW)          | 1.0/3.0          | 20 $\mu A$ / -1.8 mA                            |
| $Q_1, Q_2, \bar{Q}_1, \bar{Q}_2$ | Outputs                                 | 50/33.3          | -1 mA/20 mA                                     |

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## Truth Table

| Inputs      |             |    |   |           | Outputs |             |
|-------------|-------------|----|---|-----------|---------|-------------|
| $\bar{S}_D$ | $\bar{C}_D$ | CP | J | $\bar{K}$ | Q       | $\bar{Q}$   |
| L           | H           | X  | X | X         | H       | L           |
| H           | L           | X  | X | X         | L       | H           |
| L           | L           | X  | X | X         | H       | H           |
| H           | H           | ↗  | l | l         | L       | H           |
| H           | H           | ↗  | h | l         | Toggle  |             |
| H           | H           | ↗  | l | h         | $Q_0$   | $\bar{Q}_0$ |
| H           | H           | ↗  | h | h         | H       | L           |
| H           | H           | L  | X | X         | $Q_0$   | $\bar{Q}_0$ |

H (h) = HIGH Voltage Level

L (l) = LOW Voltage Level

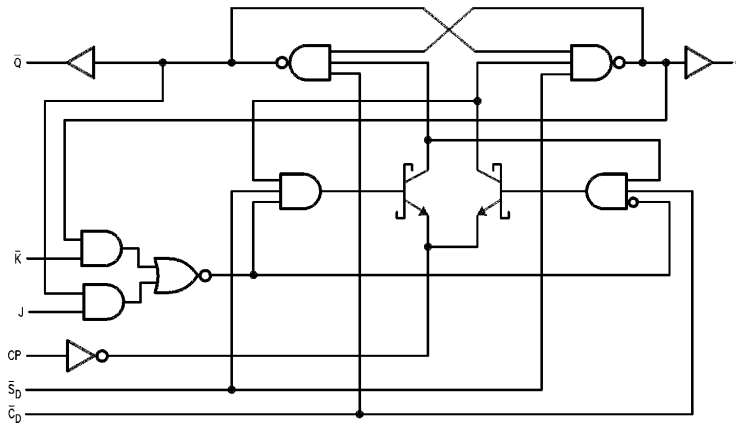
↗ = LOW-to-HIGH Transition

X = Immaterial

$Q_0$  ( $\bar{Q}_0$ ) = Before LOW-to-HIGH Transition of Clock

Lower case letters indicate the state of the referenced output one setup time prior to the LOW-to-HIGH clock transition.

# **Logic Diagram** (One Half Shown)



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Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings (Note 3)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|   |                          |
|---|--------------------------|
| Storage Temperature   | –65°C to +150°C          |
| Ambient Temperature under Bias                                      | –55°C to +125°C          |
| Junction Temperature under Bias                                     | –55°C to +175°C          |
| Plastic   | –55°C to +150°C          |
| V <sub>CC</sub> Pin Potential to Ground Pin                         | –0.5V to +7.0V           |
| Input Voltage (Note 4)  | –0.5V to +7.0V           |
| Input Current (Note 4)  | –30 mA to +5.0 mA        |
| Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V) |                          |
| Standard Output   | –0.5V to V <sub>CC</sub> |
| TRI-STATE® Output   | –0.5V to +5.5V           |

|  |                                      |
|--|--------------------------------------|
| Current Applied to Output in LOW State (Max) | twice the rated I <sub>OL</sub> (mA) |
| ESD Last Passing Voltage (Min)               | 4000V                                |

## Recommended Operating Conditions

|                              |                 |
|------------------------------|-----------------|
| Free Air Ambient Temperature |                 |
| Military                     | –55°C to +125°C |
| Commercial                   | 0°C to +70°C    |
| Supply Voltage               |                 |
| Military                     | +4.5V to +5.5V  |
| Commercial                   | +4.5V to +5.5V  |

**Note 3:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

**Note 4:** Either voltage limit or current limit is sufficient to protect inputs.

## DC Electrical Characteristics

| Symbol           | Parameter                         |                         | 54F/74F |      |      | Units | V <sub>CC</sub> | Conditions   |
|------------------|-----------------------------------|-------------------------|---------|------|------|-------|-----------------|--|
|                  |                                   |                         | Min     | Typ  | Max  |       |                 |  |
| V <sub>IH</sub>  | Input HIGH Voltage                |                         | 2.0     |      |      | V     |                 | Recognized as a HIGH Signal                                |
| V <sub>IL</sub>  | Input LOW Voltage                 |                         |         |      | 0.8  | V     |                 | Recognized as a LOW Signal                                 |
| V <sub>CD</sub>  | Input Clamp Diode Voltage         |                         |         |      | –1.2 | V     | Min             | I <sub>IN</sub> = –18 mA                                   |
| V <sub>OH</sub>  | Output HIGH Voltage               | 54F 10% V <sub>CC</sub> | 2.5     |      |      | V     | Min             | I <sub>OH</sub> = –1 mA                                    |
|                  |                                   | 74F 10% V <sub>CC</sub> | 2.5     |      |      |       |                 | I <sub>OH</sub> = –1 mA                                    |
|                  |                                   | 74F 5% V <sub>CC</sub>  | 2.7     |      |      |       |                 | I <sub>OH</sub> = –1 mA                                    |
| V <sub>OL</sub>  | Output LOW Voltage                | 54F 10% V <sub>CC</sub> |         |      | 0.5  | V     | Min             | I <sub>OL</sub> = 20 mA                                    |
|                  |                                   | 74F 10% V <sub>CC</sub> |         |      | 0.5  |       |                 | I <sub>OL</sub> = 20 mA                                    |
| I <sub>IH</sub>  | Input HIGH Current                | 54F                     |         |      | 20.0 | μA    | Max             | V <sub>IN</sub> = 2.7V                                     |
|                  |                                   | 74F                     |         |      | 5.0  |       |                 |  |
| I <sub>BVI</sub> | Input HIGH Current Breakdown Test | 54F                     |         |      | 100  | μA    | Max             | V <sub>IN</sub> = 7.0V                                     |
|                  |                                   | 74F                     |         |      | 7.0  |       |                 |  |
| I <sub>CEX</sub> | Output HIGH Leakage Current       | 54F                     |         |      | 250  | μA    | Max             | V <sub>OUT</sub> = V <sub>CC</sub>                         |
|                  |                                   | 74F                     |         |      | 50   |       |                 |  |
| V <sub>ID</sub>  | Input Leakage Test                | 74F                     | 4.75    |      |      | V     | 0.0             | I <sub>ID</sub> = 1.9 μA<br>All Other Pins Grounded        |
| I <sub>OD</sub>  | Output Leakage Circuit Current    | 74F                     |         |      | 3.75 | μA    | 0.0             | V <sub>IOD</sub> = 150 mV<br>All Other Pins Grounded       |
| I <sub>IL</sub>  | Input LOW Current                 |                         |         |      | –0.6 | mA    | Max             | V <sub>IN</sub> = 0.5V (J <sub>n</sub> , $\bar{K}_n$ )     |
|                  |                                   |                         |         |      | –1.8 |       | Max             | V <sub>IN</sub> = 0.5V ( $\bar{C}_{Dn}$ , $\bar{S}_{Dn}$ ) |
| I <sub>OS</sub>  | Output Short-Circuit Current      |                         | –60     |      | –150 | mA    | Max             | V <sub>OUT</sub> = 0V                                      |
| I <sub>CC</sub>  | Power Supply Current              |                         |         | 11.7 | 17.0 | mA    | Max             | CP = 0V  |

## AC Electrical Characteristics

See Section 0 for Waveforms and Load Configurations

| Symbol           | Parameter               | 74F   |     |     | 54F  |     | 74F  |     | Units | Fig. No. |
|------------------|-------------------------|---|-----|-----|--|-----|--|-----|-------|----------|
|                  |                         | T <sub>A</sub> = +25°C<br>V <sub>CC</sub> = +5.0V<br>C <sub>L</sub> = 50 pF |     |     | T <sub>A</sub> , V <sub>CC</sub> = Mil<br>C <sub>L</sub> = 50 pF |     | T <sub>A</sub> , V <sub>CC</sub> = Com<br>C <sub>L</sub> = 50 pF |     |       |          |
|                  |                         | Min   | Typ | Max | Min  | Max | Min  | Max |       |          |
| f <sub>max</sub> | Maximum Clock Frequency | 100   | 125 |     | 70   |     | 90   |     | MHz   | ◆◆◆◆     |

## AC Electrical Characteristics (Continued)

See Section 0 for Waveforms and Load Configurations

| Symbol    | Parameter   | 74F  |     |     | 54F  |      | 74F  |      | Units | Fig. No. |
|-----------|---|--|-----|-----|--|------|--|------|-------|----------|
|           |   | $T_A = +25^{\circ}\text{C}$<br>$V_{CC} = +5.0\text{V}$<br>$C_L = 50\text{ pF}$ |     |     | $T_A, V_{CC} = \text{Mil}$<br>$C_L = 50\text{ pF}$ |      | $T_A, V_{CC} = \text{Com}$<br>$C_L = 50\text{ pF}$ |      |       |          |
|           |   | Min  | Typ | Max | Min  | Max  | Min  | Max  |       |          |
| $t_{PLH}$ | Propagation Delay   | 3.8  | 5.3 | 7.0 | 3.8  | 9.0  | 3.8  | 8.0  | ns    | ◆◆◆◆     |
| $t_{PHL}$ | $CP_n$ to $Q_n$ or $\overline{Q}_n$                                     | 4.4  | 6.2 | 8.0 | 4.4  | 10.5 | 4.4  | 9.2  |       |          |
| $t_{PLH}$ | Propagation Delay   | 3.2  | 5.2 | 7.0 | 3.2  | 9.0  | 3.2  | 8.0  |       |          |
| $t_{PHL}$ | $\overline{C}_{Dn}$ or $\overline{S}_{Dn}$ to $Q_n$ or $\overline{Q}_n$ | 3.5  | 7.0 | 9.0 | 3.5  | 11.5 | 3.5  | 10.5 | ns    | ◆◆◆◆     |

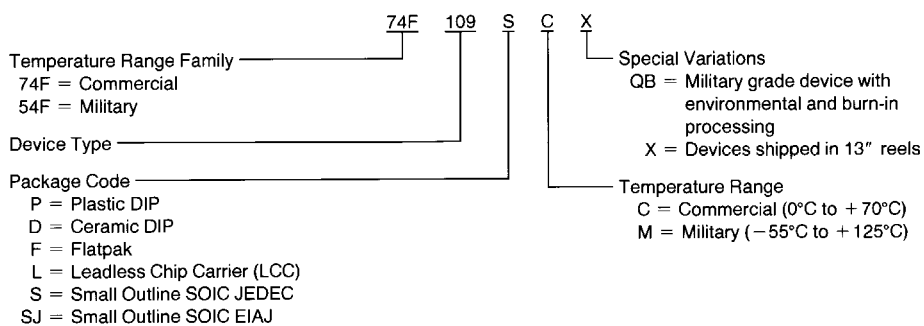
## AC Operating Requirements

See Section 0 for Waveforms

| Symbol           | Parameter   | 74F  |     | 54F                        |     | 74F                        |     | Units | Fig. No. |
|------------------|---|--|-----|----------------------------|-----|----------------------------|-----|-------|----------|
|                  |   | $T_A = +25^{\circ}\text{C}$<br>$V_{CC} = +5.0\text{V}$ |     | $T_A, V_{CC} = \text{Mil}$ |     | $T_A, V_{CC} = \text{Com}$ |     |       |          |
|                  |   | Min  | Max | Min                        | Max | Min                        | Max |       |          |
| $t_s(\text{H})$  | Setup Time, HIGH or LOW   | 3.0  |     | 3.0                        |     | 3.0                        |     | ns    | ◆◆◆◆     |
| $t_s(\text{L})$  | $J_n$ or $\overline{K}_n$ to $\text{CP}_n$  | 3.0  |     | 4.0                        |     | 3.0                        |     |       |          |
| $t_h(\text{H})$  | Hold Time, HIGH or LOW  | 1.0  |     | 1.0                        |     | 1.0                        |     |       |          |
| $t_h(\text{L})$  | $J_n$ or $\overline{K}_n$ to $\text{CP}_n$  | 1.0  |     | 1.0                        |     | 1.0                        |     |       |          |
| $t_w(\text{H})$  | $\text{CP}_n$ Pulse Width   | 4.0  |     | 4.0                        |     | 4.0                        |     | ns    | ◆◆◆◆     |
| $t_w(\text{L})$  | HIGH or LOW   | 5.0  |     | 5.0                        |     | 5.0                        |     |       |          |
| $t_w(\text{L})$  | $\overline{\text{C}}_{\text{Dn}}$ or $\overline{\text{S}}_{\text{Dn}}$ Pulse Width, LOW       | 4.0  |     | 4.0                        |     | 4.0                        |     | ns    | ◆◆◆◆     |
| $t_{\text{rec}}$ | Recovery Time<br>$\overline{\text{C}}_{\text{Dn}}$ or $\overline{\text{S}}_{\text{Dn}}$ to CP | 2.0  |     | 2.0                        |     | 2.0                        |     | ns    | ◆◆◆◆     |

## Ordering Information

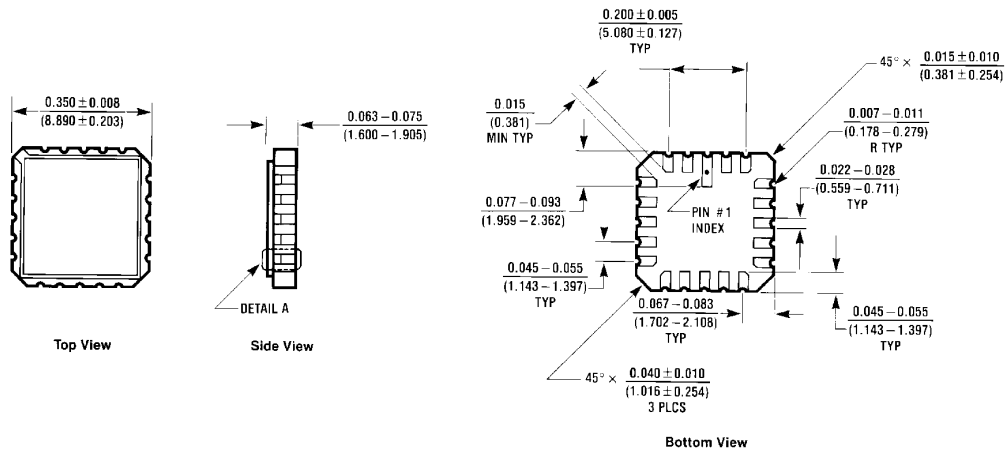
The device number is used to form part of a simplified purchasing code where the package type and temperature range are defined as follows:



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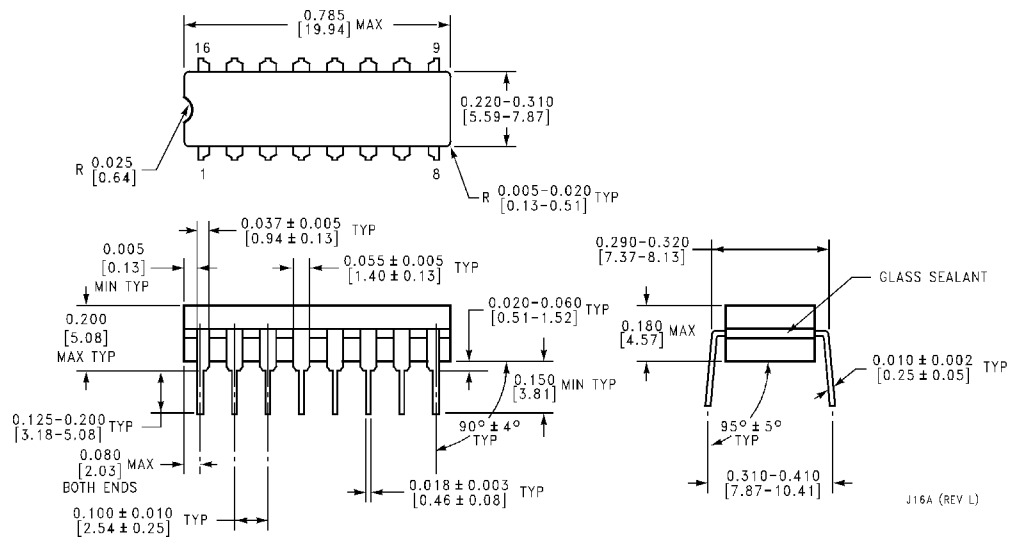


# Physical Dimensions inches (millimeters) unless otherwise noted



**20-Lead Ceramic Leadless Chip Carrier (L)**  
**NS Package Number E20A**

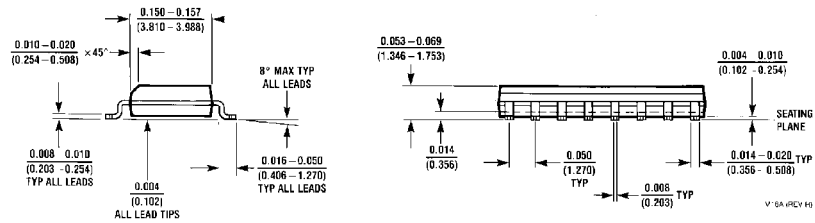
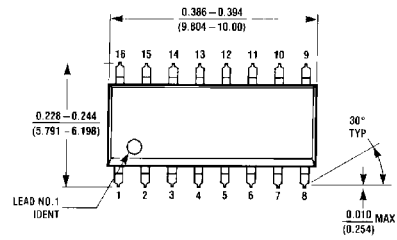
E20A (REV D)



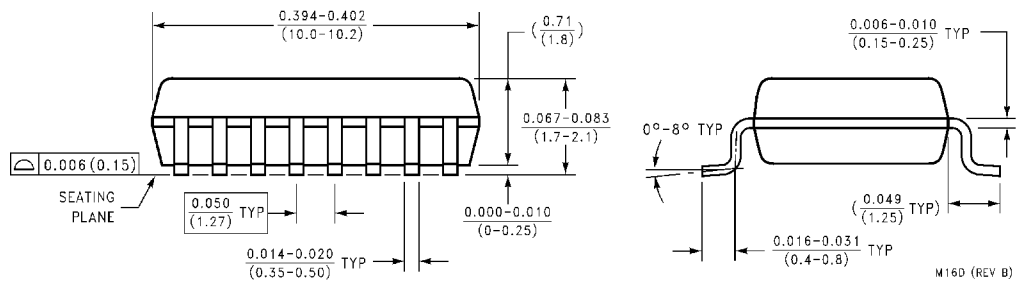
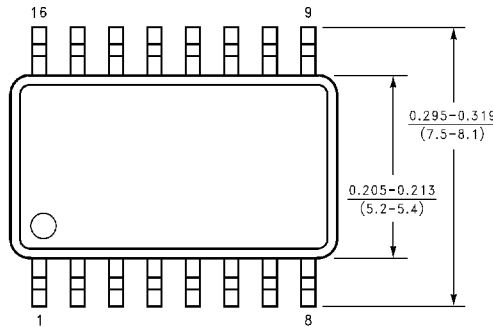
**16-Lead Ceramic Dual-In-Line Package (D)**  
**NS Package Number J16A**

J16A (REV L)

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



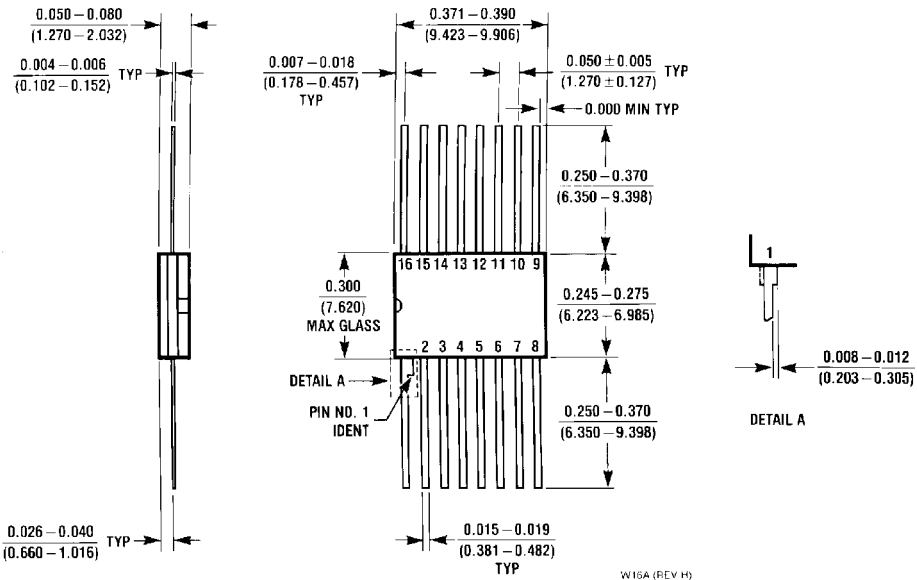
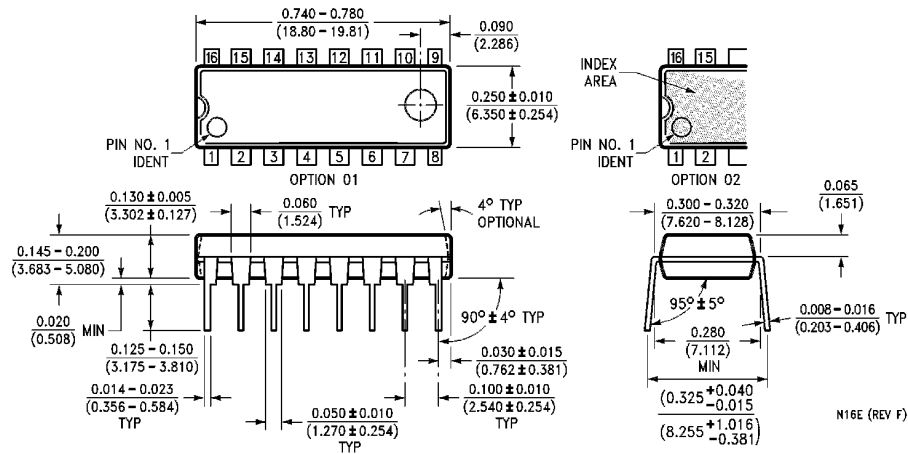
**16-Lead (0.150" Wide) Molded Small Outline Package, JEDEC (S)  
NS Package Number M16A**



**16-Lead (0.300" Wide) Molded Small Outline Package, EIAJ (SJ)  
NS Package Number M16D**



**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



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